UNIVERSITÉ DE SHERBROOKE

3D Monolithic integration of Schottky Barrier FET on a CMOS circuit

Ph.D. project

Intel or Samsung are currently manufacturing high volumes of 14 nm processors and their future 7 nm generation finFETs are already in the development phase for production. It is anticipated that this CMOS scaling trend will ultimately result in 5-7 nm gate transistors. Tremendous research efforts are thus ongoing in order to fulfill the needs of aggressively scaled transistors, new materials, and architectures that are introduced in almost every generation of integrated circuits.. With further decrease of dimensions, devices physical limitations but also energy dissipation issues will be reached. The devices integration in the circuit third dimension, the so-called 3D integration, will help increasing circuit performances by increasing the device density and system functionalities by adding new devices on top of existing CMOS. High performance and/or low power devices compatible with back-end-of-line (BEOL) 3D monolithic integration are essential technologies for the future generations of integrated circuits with demanding computing performances, large storage capacity and/or novel functionalities.
The proposed PhD project deals with the fabrication and simulation of devices and their 3D monolithic integration on a CMOS circuit. The research will focus on 3 main aspects: i) TCAD simulation of devices using different active materials and architectures including Schottky Barrier devices to evaluate the transistors performances and potential for 3D integration; ii) fabrication of devices compatible with 3D integration using state-of-the-art clean room fabrication tools; iii) modeling and 3D integration of hybrid circuits.

The Interdisciplinary Institute for Technological Innovation (3IT) hosts a concentration of academical and industrial expertise at Sherbrooke University (UdeS). This is particularly true in the frame of the reinforced partnerships between UdeS, IBM Canada and TELEDYNE Dalsa through the C2Mi MiQro Innovation Collaborative Centre, and with ST Microelectronics Crolles through the common lab LN2-ST. In the 3IT, the 850 m^2 3IT.nano clean rooms have state-of-the-art nanofabrication tools.

Requirements

- Master degree in electrical engineering or equivalent.
- Good knowledge of nanoelectronic devices.
- Experience in clean-room fabrication is a plus.
- Good simulation skills is an asset.
- Team worker with good communication skills.
- Fluent in French or English. Both is a plus.

Practical information

Location: 3IT, Sherbrooke, Québec, Canada
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